PENDING CLAIMS AND STATUS THEREOF

1. (original): A method of multiplying two maximally negative fractional numbers to produce a 32-bit result, comprising:

fetching operands from a source location;

performing a multiplication operation on the operands; and

detecting that a result output of the multiplication operation corresponds to a maximally negative result;

wherein the maximally negative result indicates that the operands are two maximally negative fractional numbers.

2. (original): The method according to claim 1, further comprising the step of correcting the result output to produce a maximally positive result output.

3. (original): The method according to claim 2, wherein the step of detecting that the result output of the multiplication operation corresponds to a maximally negative result includes the step of examining bits in a set of bits representing the result output.

4. (original): The method according to claim 3, wherein the step of detecting that the result output of the multiplication operation corresponds to a maximally negative result includes the step of determining that the bits in the set of bits representing the result have a particular bit combination.

5. **(currently amended):** The method according to claim 4, wherein the bits in the set of bits are the ~~**thirtieth and thirty-first**~~ **two most significant** bits in the set of bits representing the result output.

6. (original): The method according to claim 4, wherein the particular bit combination for the bits in the set of bits representing the result output is one and zero respectively.

7. (original): The method according to claim 2, wherein the step of correcting the result to produce a maximally positive result includes the step of generating a control signal.

8. (original): The method according to claim 7, wherein the step of correcting the result to produce a maximally positive result includes the step of modifying a negate control signal based on the control signal.

9. (original): The method according to claim 8, wherein the step of correcting the result to produce a maximally positive result includes the step of performing a two's compliment on the result output.

10. (original): The method according to claim 9, further comprising:

accumulating the maximally positive result output to an accumulator.

11. (original): The method according to claim 1, further comprising the step of fractionally aligning the result output.

12. (original): The method according to claim 11, wherein the step of fractionally aligning the result output includes the step of shifting a set of bits representing the result output to the left by one bit to discard the most significant bit of the set of bits representing the result output and insert a zero as the least significant bit of the set of bits representing the result output.

13. (original): The method according to claim 1, further comprising the step of sign extending the output result.

14. (original): The method according to claim 13, wherein the result output is extended from a 32-bit result to a 40-bit result.

15. (original): A processor for multiplication operation instruction processing, comprising:

a DSP unit operable to:

fetch operands from a source location;

perform a multiplication operation on the operands; and

a control block operable to detect that a result output of the multiplication operation corresponds to a maximally negative result;

wherein the maximally negative result indicates that the operands are two maximally negative fractional numbers.

16. (original): The processor according to claim 15, further comprising a negate logic operable to correct the result output to produce a maximally positive result output.

17. (original): The processor according to claim 16, wherein the control block detects a maximally negative result by examining bits in a set of bits representing the result output.

18. (original): The processor according to claim 17, wherein the examination of the bits in the set of bits is to determine a particular bit combination.

19. **(currently amended):** The processor according to claim 18, wherein the bits in the set of bits are the ~~**thirtieth and thirty-first**~~ **two most significant** bits in the set of bits representing the result output.

20. (original): The processor according to claim 18, wherein the particular bit combination for the bits in the set of bits representing the result output is one and zero respectively.

21. (original): The processor according to claim 16, wherein the control block generates a control signal.

22. (original): The processor according to claim 21, wherein the control signal is operable to modify a negate control signal.

23. (original): The processor according to claim 22, wherein the negate logic is operable to perform a two's compliment operation on the result output based on the negate control signal.

24. (original): The processor according to claim 23, further comprising:

an accumulator operable to accumulate the maximally positive result output.

25. (original): The processor according to claim 15, further comprising fractionally aligning logic operable to fractionally align the result output.

26. (original): The processor according to claim 25, wherein the fractionally alignment logic shifts a set of bits representing the result output to the left by one bit to discard

the most significant bit of the set of bits representing the result output and insert a zero as the least significant bit of the set of bits representing the result output.

27. (original): The processor according to claim 15, further comprising sign extension logic operable to sign extend the result output.

28. (original): The processor according to claim 27, wherein the sign extension logic extends the result output from a 32-bit result to a 40-bit result.